



UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/566,813	01/30/2006	David Casey	0789860222	8053

23392 7590 12/28/2007
FOLEY & LARDNER
2029 CENTURY PARK EAST
SUITE 3500
LOS ANGELES, CA 90067

EXAMINER

LEE, JAE

ART UNIT	PAPER NUMBER
----------	--------------

2823

MAIL DATE	DELIVERY MODE
-----------	---------------

12/28/2007

PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary

Application No.

10/566,813

Applicant(s)

CASEY, DAVID

Examiner

Jae Lee

Art Unit

2823

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --
Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 08 October 2007.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-5, 7 and 8 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-5, 7, 8 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
- ☐ Certified copies of the priority documents have been received.
 - ☐ Certified copies of the priority documents have been received in Application No. _____.
 - ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|---|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413) |
| 2) <input type="checkbox"/> Notice of Draftperson's Patent Drawing Review (PTO-948) | Paper No(s)/Mail Date. _____ |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO/SB/08) | 5) <input type="checkbox"/> Notice of Informal Patent Application |
| Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____ |

DETAILED ACTION

Response to Arguments

1. Applicant's arguments, see pages 6-7, filed 10/08/2007, with respect to the rejection(s) of claim(s) 1-5 under Palara have been fully considered and are persuasive. Therefore, the rejection has been withdrawn. However, upon further consideration, a new ground(s) of rejection is made in view of Singh (Pub No. US 2005/0269633 A1, hereinafter Singh).

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

3. The text of those sections of Title 35, U.S. Code not included in this action can be found in a prior Office action.

4. **Claims 1-5,7,8** are rejected under 35 U.S.C. 103(a) as being unpatentable over Palara in view of Singh.

With regards to **claim 1**, Palara teaches a bipolar transistor, comprising:

A first semiconductor region of a first conductivity type defining a collector region
(see Fig. 2, collector region 2);

a second semiconductor region of a second conductivity type defining a base region (see Fig. 2, base region 1);

a third semiconductor region of said first conductivity type defining a emitter region (see Fig. 2, emitter region **12**); and

a metal layer providing contacts to said base and emitter regions (see Fig. 2, emitting regions **8** and base regions **5**);

wherein said metal layer has a thickness greater than 3 microns (see col. 6, lines 11-12).

Palara, however, does not teach wherein the transistor has a specific area resistance less than $500 \text{ mOhms} \cdot \text{mm}^2$.

In the same field of endeavor, Singh teaches a power transistor (LDVMISFET) which has a specific on resistance of less than $300 \text{ mOhms} \cdot \text{cm}^2$ (see ¶18).

Therefore, it would have been obvious to a person having ordinary skill in the art at the time the invention was made to produce a power transistor with less than $500 \text{ mOhms} \cdot \text{mm}^2$ since it has already been made known and demonstrated by Singh

With regards to **claims 2 and 3**, Palara teaches the limitations of claim 1 for the reasons above.

Palara teaches the thickness of the metal layer is $3 \mu\text{m}$ (see col. 6, lines 11-12).

Palara does not teach a bipolar transistor according to **claim 1**, wherein the metal layer has a thickness no less than $4 \mu\text{m}$.

Palara does not teach a bipolar transistor according to **claim 1**, wherein the metal layer no less than $6 \mu\text{m}$.

In the same field of endeavor, it would have been obvious to one of ordinary skill to determine the optimum the thickness of the metal layer (see In re Aller, Lacey, and Hall (10 USPQ 233-237). It is not inventive to discover the optimum or workable ranges by routine experimentation. Note that the specification contains no disclosure of either the critical nature of the claimed ranges or any unexpected results arising therefrom. Where patentability is said to be based upon particular chosen dimensions or upon another variable recited in a claim, the applicant must show that the chosen dimensions are critical (see In re Woodruff, 919 f.2d 1575, 1578, 16USPQ 2d, 1934, 1936 (Fed. Cir. 1990)).

With regards to **claim 4**, Palara teaches a bipolar transistor according to **claim 1**, wherein the emitter region defines a first surface, the base region extending to said surface in locations defined by apertures through emitter region, said metal layer overlying said first surface (see Fig. 7, emitter region **12** define surface, base region **1** extending to surface, apertures (alternating **8** and **5**) through emitter region **12**, regions **8** and **5** composed of metal layer overlying surface).

With regards to **claim 5**, Palara teaches the limitations of claim 4 for the reasons above.

Palara, however, does not teach a bipolar transistor according to **claim 4**, wherein adjacent apertures are spaced less than 100 μm from each other.

In the same field of endeavor, it would have been obvious to one of ordinary skill to determine the optimum distance between two apertures (see In re Aller, Lacey, and Hall (10 USPQ 233-237)). It is not inventive to discover the optimum or workable ranges by routine experimentation. Note that the specification contains no disclosure of either the critical nature of the claimed ranges or any unexpected results arising therefrom. Where patentability is said to be based upon particular chosen dimensions or upon another variable recited in a claim, the applicant must show that the chosen dimensions are critical (see In re Woodruff, 919 F.2d 1575, 1578, 16 USPQ 2d, 1934, 1936 (Fed. Cir. 1990)).

With regards to **claim 7**, Palara and Singh does not teach the bipolar transistor according to **claim 1**, wherein an increase in the thickness of the metal layer corresponds to a reduction in a voltage drop in the contacts to said base and emitter region.

In the same field of endeavor, it is obvious to a person having ordinary skill in the art at the time the invention was made to realize that an increase in thickness of the metal layer will inherently create a reduction in a voltage drop. That is simply known and inherent to the semiconductor industry that the voltage will not drop as much with a thicker metal layer since the resistance is lowered.

With regards to **claim 8**, Palara and Singh does not teach the bipolar transistor according to **claim 7**, wherein the reduction in the voltage drop in the contacts is proportional to the increase in the thickness of the metal layer.

In the same field of endeavor, it is obvious to a person having ordinary skill in the art at the time the invention was made to realize that there is a mathematical relationship between the reduction in voltage drop and an increase in the thickness of the metal layer.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jae Lee whose telephone number is 571-270-1224. The examiner can normally be reached on Monday - Friday, 7:30 a.m. - 5:00 p.m. EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matthew Smith can be reached on 571-272-1907. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Application/Control Number:
10/566,813
Art Unit: 2823

Page 7

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

JML




LEX MALSAWMA
PRIMARY PATENT EXAMINER